Ultra-low Power Sentry for Ambient Powered Smart Sensors

Final Report

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Basic Circuit Operation

The basic circuit operation of the power sentry system was presented previously in the 3rd Quarterly Report, but it has been updated and included again as a reminder. The proposed power sentry system requires several components to realize the signal processing technique for monitoring a sensor output to detect the presence of signals with defined frequency and amplitude properties. In this section, each component's role within the system will be described to provide a general understanding of how the implemented circuit design performs the desired function. The circuit that was designed and implemented during the first two quarters of the project is seen in Figure (1).
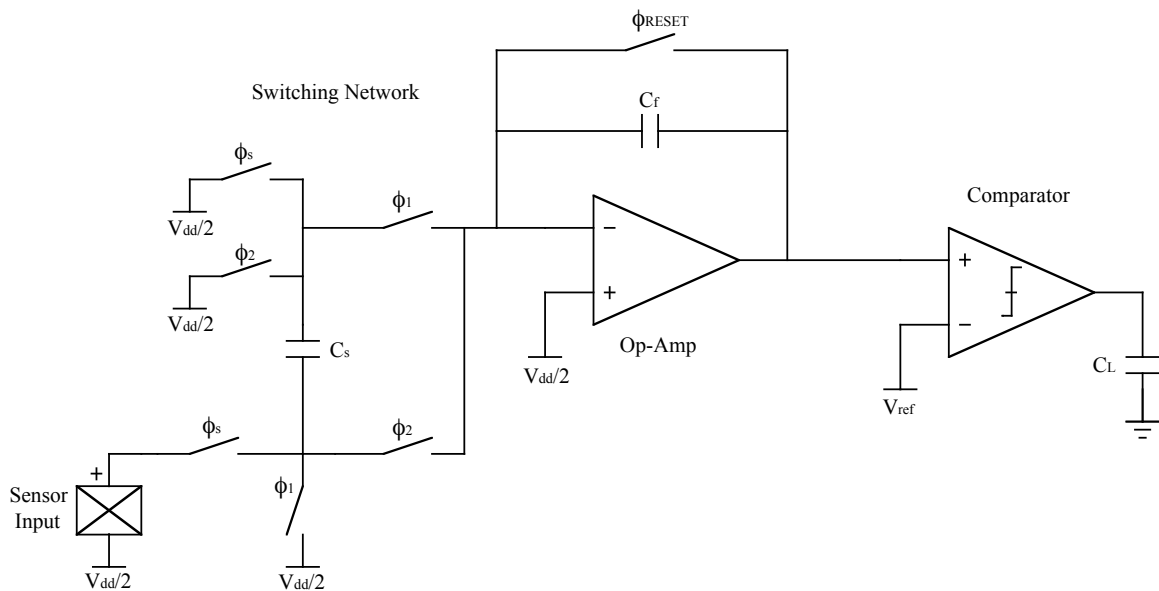

Figure 1: Sentry system

The input sensor is connected to a sampling capacitor, C_s, through the integrated switching network. The clock divider circuitry controls the switching network, which is internal to the circuit design. In tandem, the clock divider and switching network are used to implement a modulation of the input signal with the Hadamard basis functions that is critical to the signal processing aspect of the sentry system. The reason for using the Hadamard function implementation is due to the fact that passive narrow-band analog filters require

complex networks of components, which makes them very inflexible. However, the proposed circuit implementing the Hadamard function method is rather flexible. A simple switched-capacitor integrator network implements the desired Hadamard functions. This switched-capacitor network generates the necessary Hadamard basis functions described below, which allow the designer to determine which frequencies in the spectrum are being examined by the sentry system. The frequencies under examination are determined by the selected Hadamard basis function and the switching network sampling frequency. The design proposed herein is capable of monitoring the input signal at the frequencies f_s, $f_s/2$, and $f_s/4$.

The clock divider operates such that a single clock signal is applied to the circuit and the necessary clocks – ϕ_s, ϕ_1, and ϕ_2 – are generated within. In order to select which Hadamard basis function – H_1, H_2, or H_3 – is implemented for detection of a particular frequency, two user-controlled select lines are provided. The sub-set of Hadamard basis functions is defined in Eqs. (1), where N represents the resolution of the performed computations.

$$H_1 = [1, 1, 1, 1, \ldots]_{1xN} \tag{1a}$$

$$H_2 = [1, -1, 1, -1, \ldots]_{1xN} \tag{1b}$$

$$H_3 = [1, 1, -1, -1, \ldots]_{1xN} \tag{1c}$$

These basis functions control how the input signal from the sensor is sampled and transferred to the op-amp (integrator). It is important to note that the clock divider is implemented such that the sampling frequency will always be half the frequency of the input clock frequency. Additionally, the clock signals, ϕ_s, ϕ_1, and ϕ_2, are generated such that they are guaranteed to be non-overlapping. This is important to ensure that the operation of the sentry system is as expected.

The op-amp is used to implement the integrator structure needed to calculate the Hadamard coefficients defined by Eq. (2),

$$X_{H_k} = \sum_{n=0}^{N-1} x[n] \cdot H_k[n] \tag{2}$$

where x[n] are the input samples taken from the sensor and $H_k[n]$ are the Hadamard basis functions defined in Eq. (1). Since the Hadamard basis functions are composed solely of 1 and –1, the integrator needs to perform sign alternation (when necessary) of the input samples and summation. The previously described clock divider and switching network effectively implement $x[n] \cdot H_k[n]$ from Eq. (2), which is the necessary sign alternation function. Thus, the integrator must only perform summation, which is simply integration with a reset function. This is implemented by including the switch in the integrator feedback path that is controlled by the signal ϕ_{RESET}. The frequency resolution is controlled by the number of samples, N, integrated during computation of X_{H_k}. The more samples integrated, the finer the frequency resolution. This resolution is defined in Eq. (3) as the –3 dB bandwidth (BW).

$$BW \cong \frac{0.6 \cdot f_s}{N} \qquad\qquad (3)$$

The –3 dB BW equation allows the sensor network designer to predict which frequencies will be included in the computation of the particular Hadamard coefficient when checking for the presence of an expected frequency.

The final component of the design is the comparator, or quantizer. The comparator is used to determine the absence or presence of a signal at the particular frequency of interest. This detection requires some prior knowledge of the environment the sensor is in, and also, it requires prior knowledge of the sensor's behavior. In order to determine whether or not a signal is present at a given frequency, the comparator must determine if the integrator output is above or below the spectrum noise floor. The comparator output is controlled by a latch signal, V_{latch}, which may be asserted once the N-sample integration is complete. When the signal V_{latch} is low, the comparator output is pulled to V_{dd}. However, when V_{latch} is asserted, the comparator outputs a digital '1' if the input is above the reference voltage V_{ref} or a digital '0' if the input is below V_{ref}. At this point, the sentry system determined whether or not an actual signal at the particular frequency of interest is present in the signal spectrum.

Experimental Results from Fabricated Chip

This section presents the experimental results of the individual components that were fabricated using the AMIS 1.5μm CMOS process. The functionality of each component will be verified and resulting performance criteria will be discussed. Most importantly, accurate power measurements will be provided for these components since that is the critical metric for the sentry system.

The first component to be analyzed is the clock generator circuitry. The clock generator provides the necessary clock signals to select which frequency band will be examined for the presence or absence of a signal through the use of Hadamard basis functions. The Hadamard basis function selection is performed according to the external select lines (Sel_1 and Sel_2) provided as inputs to the chip and is described in Table 1.

Sel_1	Sel_2	Hadamard Basis Function
0	0	H_1
0	1	H_2
1	0	H_1
1	1	H_3

Table 1: Hadamard basis function selection

The following figures – Figure (2), Figure (3), and Figure (4) – display the clock functions generated by the IC for the different Hadamard basis functions – H_1, H_2, and H_3 – respectively. The signals shown in each figure are displayed from top to bottom in the order: input clock, ϕ_s, ϕ_1, and ϕ_2 (where applicable). As seen in the figures, the clock signals were designed so that they were guaranteed to be non-overlapping. This is essential to guarantee accuracy of the charge sampling and transferring operations performed by the switching network. When the clock signals are applied to the circuit shown in Figure (1), the necessary

sign alternations of the sampled sensor input signal and charge transfers are performed as expected.

The average current consumption for each Hadamard basis function generation is shown in Table 2. As seen in the table, the average current is quite low for each basis function, and each is within the current budget allotted in the first report (375nA). The worst-case power consumption for the clock divider circuitry is thus the supply voltage, V_{dd}, times the current for the H_2 Hadamard basis function, since this selection requires the greatest current. The result is 1.371 μW of power.
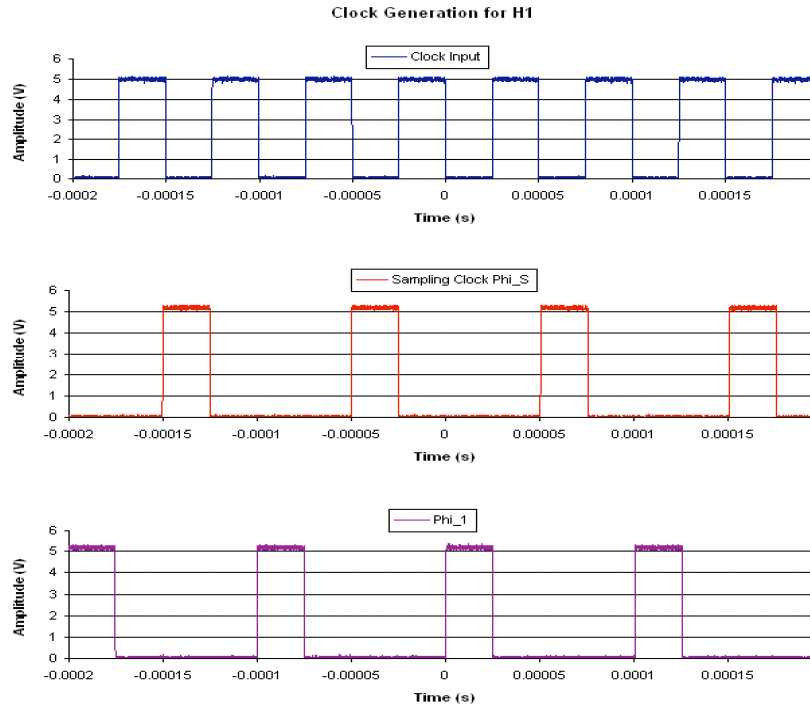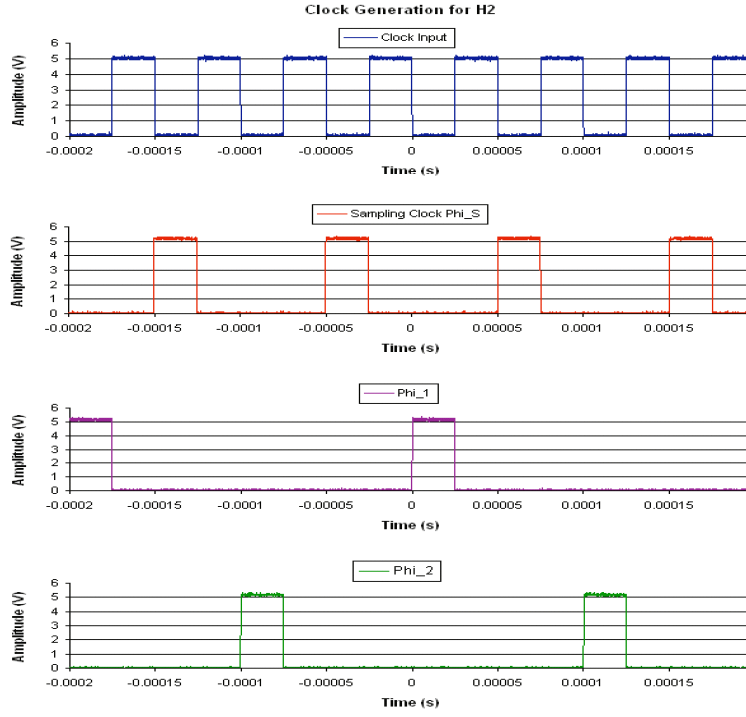

Figure 2: Hadamard basis function H_1
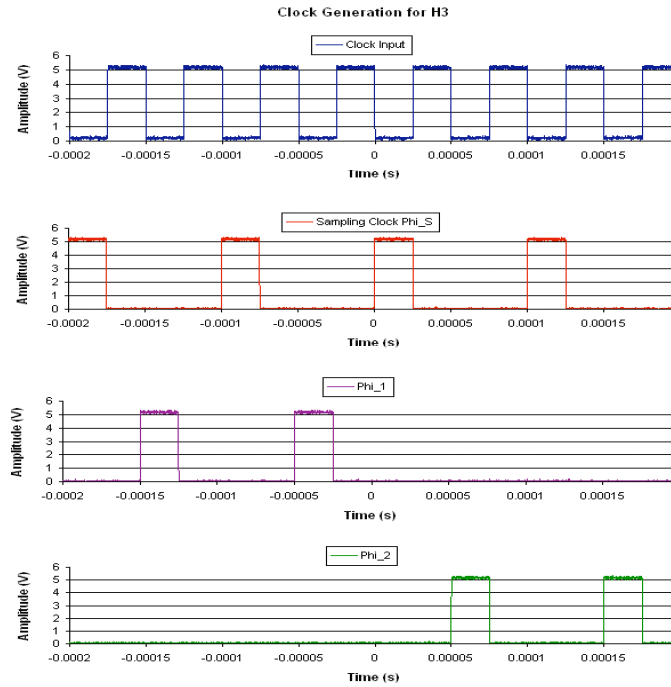
Figure 3: Hadamard basis function H$_2$

Figure 4: Hadamard basis function H$_3$

	H$_1$	H$_2$	H$_3$
I$_{ave}$	262.3 nA	274.3 nA	268.8 nA
P$_{ave}$	1.312 μW	1.371 μW	1.344 μW

Table 2: Clock Divider current consumption values

The next component of the sentry system chip to be tested is the op-amp. The op-amp's performance turned out to be slightly worse than the expected results provided by simulations. Several factors turned out to be problematic including input offsets, non-ideal transistor sizings, and, most noticeably, slew rate. Unfortunately, low bias currents, which are required for the low total current consumption of the op-amp, force the op-amp to become slew-rate limited before a measurement of the unity gain frequency can be obtained. The slew-rate of an operational amplifier is limited by the current source that biases the input differential pair of the amplifier. This current source limits the amount of current that can be used to charge the compensation capacitor, thus limiting the maximum rate of change of the output voltage. When the amplifier is pushed to the point that this limit is reached (i.e., the rate of change of the output voltage is higher that the slew rate), it can no longer function properly. The resulting output for a sinusoidal input to a slew-rate limited op-amp is a triangular shaped waveform. The predicted slew-rate value for the op-amp can be obtained through evaluating Eq. (4).

$$SR = \frac{I_{bias1}}{C_c} = \frac{1.15 \mu A}{3 pF} = 0.38 \frac{V}{\mu s} \tag{4}$$

The bias current, I$_{bias1}$, used in Eq. (4) is a mirrored version of the current through the op-amp's external 500k_ bias resistor. Furthermore, the current mirror is designed with a gain of ten such that the current through the first stage, I$_{bias1}$, is ten times the current through the bias resistor, I$_{bias}$. The current through the bias resistor is measured to be I$_{bias}$= 0.115μA. Thus, the current through the first stage, I$_{bias1}$, is 1.15μA. It is worth

noting that for a typical op-amp, the slew-rate value is generally a minimum of 20V/μA, and a higher slew-rate value is more desirable. The measured slew-rates, obtained through testing of the op-amp, were slightly different than the predicted value from Eq. (4). This is most likely due to process variations, which cause changes in C_c and I_{bias1}. However, these variations between measured and predicted values were within an acceptable range. The waveforms used to obtain the actual slew-rate values for the opamp can be seen in Figure (5). An inverting amplifier structure with gain A_v = -1 was used for the measurements, thus the inverted input and output waveforms. The determined slew-rate value is the slope of the triangular output waveform, which is calculated in Eq. (5). This value was determined by applying a sine wave of amplitude 0.45V to the input of the op-amp. The input waveform is also shown in Figure (5).

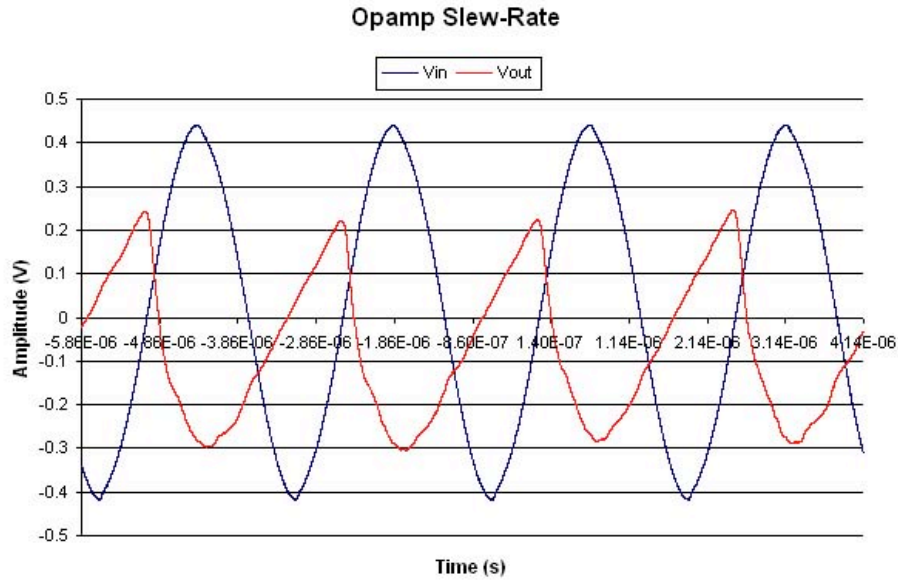$$SR = \frac{\Delta V}{\Delta t} = \frac{348mV}{1.0\mu s} = 0.348 \frac{V}{\mu s} \tag{5}$$

Figure 5: Slew-Rate waveforms

Even though the slew-rate prevented finding the true unity-gain frequency of the op-amp, the maximum frequency response was found before slew-rate limitations occurred. For the case with a 500k_ bias resistor, the op-amp was able to function up to a frequency of

20kHz without output distortions. So, for input signals below 20kHz, the op-amp should work as expected.

Another issue with the op-amp was the sizing of the current mirror transistor at the output stage. As a reminder from the 1st Quarterly Report, the op-amp circuit used in the sentry system is shown in Figure (6). When testing the functionality of the op-amp, a unity-gain inverting amplifier setup was used. To accomplish this, a resistor, R, is connected between the output terminal and the V_{in-} terminal. Additionally, a resistor of the same value is placed between the input voltage source, V_{in}, and the V_{in-} terminal. When the V_{in+} terminal is fixed at $V_{dd}/2$ and a DC voltage source is placed at V_{in}, the output is determined by Eq. (6).

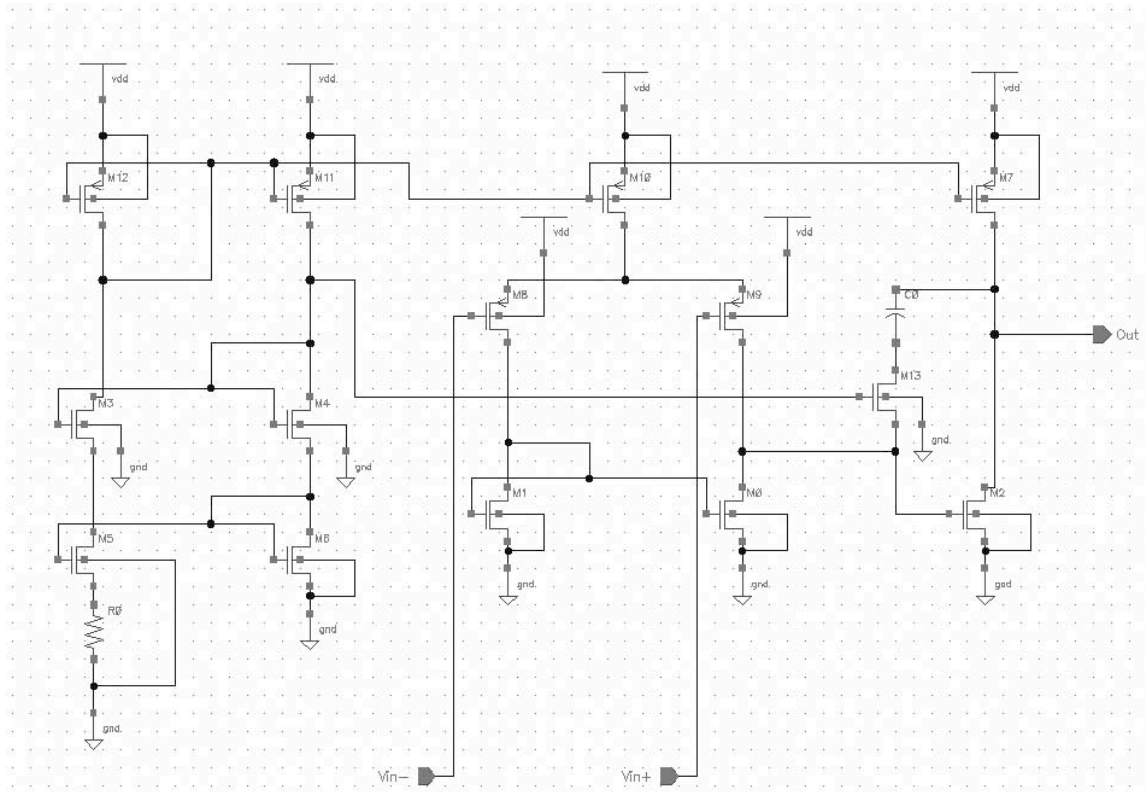$$V_{out} = 2V_{in+} - V_{in} = V_{dd} - V_{in} \qquad (6)$$
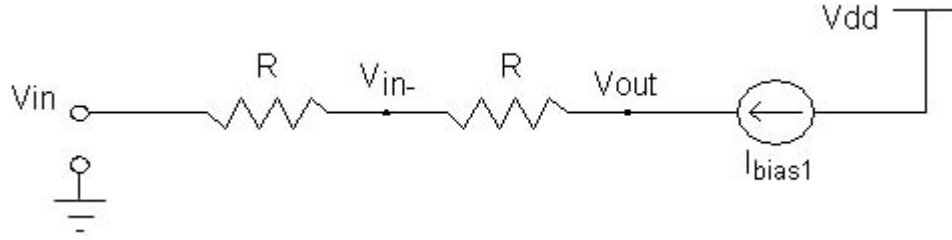

Figure 6: Op-amp schematic

Figure 7: Effective feedback created

Therefore, when an input of V_{in} = 1V is applied, V_{out} is expected to be 4V for V_{dd} = 5V and V_{ss} = 0V. However, this was not happening during testing when a 500kΩ bias resistor was used for the op-amp. What happens is that the current through the external resistors, R, used for testing the circuit reaches the saturation current through transistor M7, which supplies the current for the output stage. When this happens, transistor M2 experiences current starvation and enters the cut-off operating region. An equivalent schematic that models this behavior is shown in Figure (7). Additionally, this condition forces transistor M9 into cutoff, which makes the op-amp no longer behave as an op-amp should.

As seen in the figure, the output voltage, V_{out}, follows V_{in-}, and they decrease together. This causes the following undesirable situation to be experienced during testing. Using the setup presented above with R = 1MΩ and V_{in+} = 2.5V, the DC voltage at V_{in} is swept down from 4V to 1V. Initially, for values of V_{in} near 4V, the output was as expected (increasing linearly from 1V as the input voltage linearly decreased). However, once the input voltage reached 2.33V, the current starvation condition described above caused the output to begin decreasing instead of continuing upward to 4V as expected. Therefore, a maximum output voltage from the op-amp was determined to be 2.6V. The 0.07V deviation from the expected value was due to input offset errors, which is a common problem for single-ended op-amp designs. This test indicates that an output common-mode voltage of only 2.4V, where an extra voltage drop of 0.2V comes from the saturation voltage of transistor M2, can be achieved with this op-amp when biased using a 500kΩ resistor.

As with the other components of the power sentry system, it is important to know the power consumption of the op-amp. As mentioned previously in this section, the current through the external bias resistor was found to be 0.115µA. This current is mirrored through another branch, which sets the bias voltage for the transistor used as a resistor in the Miller compensation network between the first and second stages. The bias current is also mirrored through the input, or first amplification stage of the op-amp, but is increased ten times, resulting in a current of 1.15µA. Finally, the bias current is mirrored through the output stage, where it is eleven times the original bias current for a value of 1.265µA. Therefore, the total current consumption, $I_{op\text{-}amp}$, by the op-amp when biased using a 500k_ resistor is 2.645µA, resulting in a power consumption of V_{dd} times $I_{op\text{-}amp}$, or 13.225µW.

The final component of the sentry system to be tested was the comparator circuit. To help understand the expected comparator circuit operation, Figure (8) presents the comparator design.
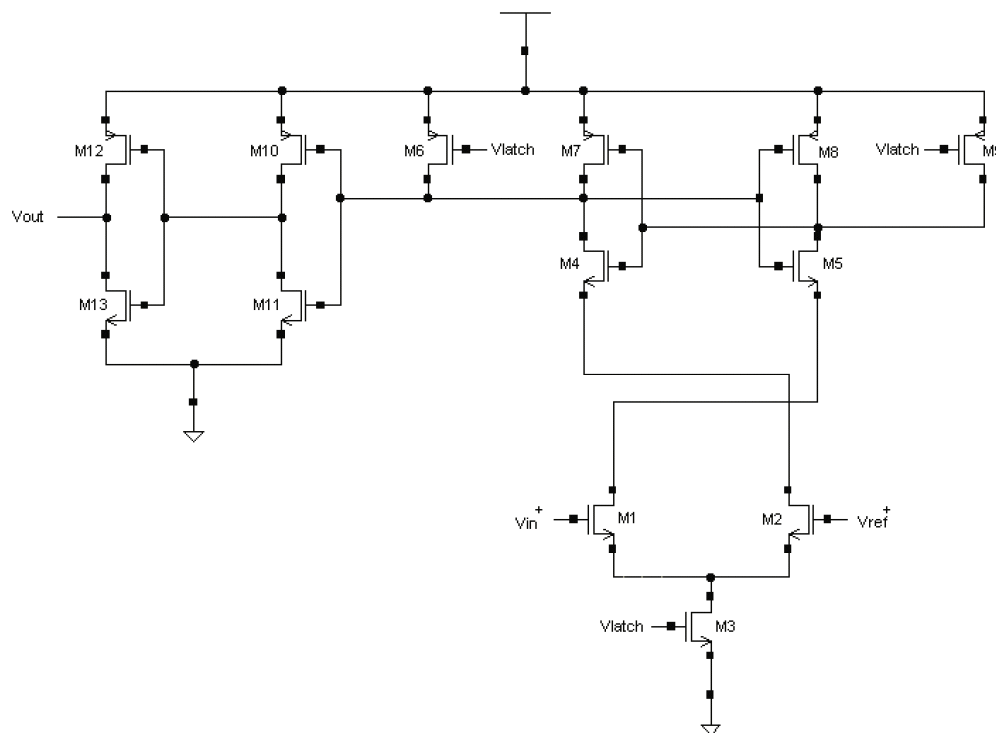

Figure 8: Comparator schematic

In order to test the basic functionality of the comparator, the following setup was used. At the input, V_{in+}, a DC voltage source is applied, where the voltage is swept from the circuit's lowest potential to its highest potential. Additionally, a square wave signal is applied to V_{latch}, which determines when the output of the comparator is to be evaluated. When V_{latch} is low, PMOS transistors M6 and M9 have their drain instantly tied to V_{dd}, which causes the inverter chain to force the output to V_{dd}. On the rising edge of the latch signal, the present input voltage is compared to the reference voltage and the output is determined. When the input voltage level is below the applied reference voltage of $V_{ref} = V_{dd}/2$, or 0 V, the comparator output is pulled to the lowest potential, V_{ss}. Once the input voltage level crosses the reference voltage, V_{ref}, the output level should remain at V_{dd} when the latch signal is asserted. Figure (9) presents the results of the described test. It is difficult to tell from the plot, but V_{in} is in fact increasing in potential from -2 ms where the voltage is below V_{ref} to 2 ms where the input is above V_{ref}.

Once the circuit operation was verified, the rise and fall times of the output were found. Figure (10) presents the plot used to determine the comparator's rise time, and Figure (11) shows the fall time plot. The rise and fall time values were found to be 142 ns and 66 ns respectively.
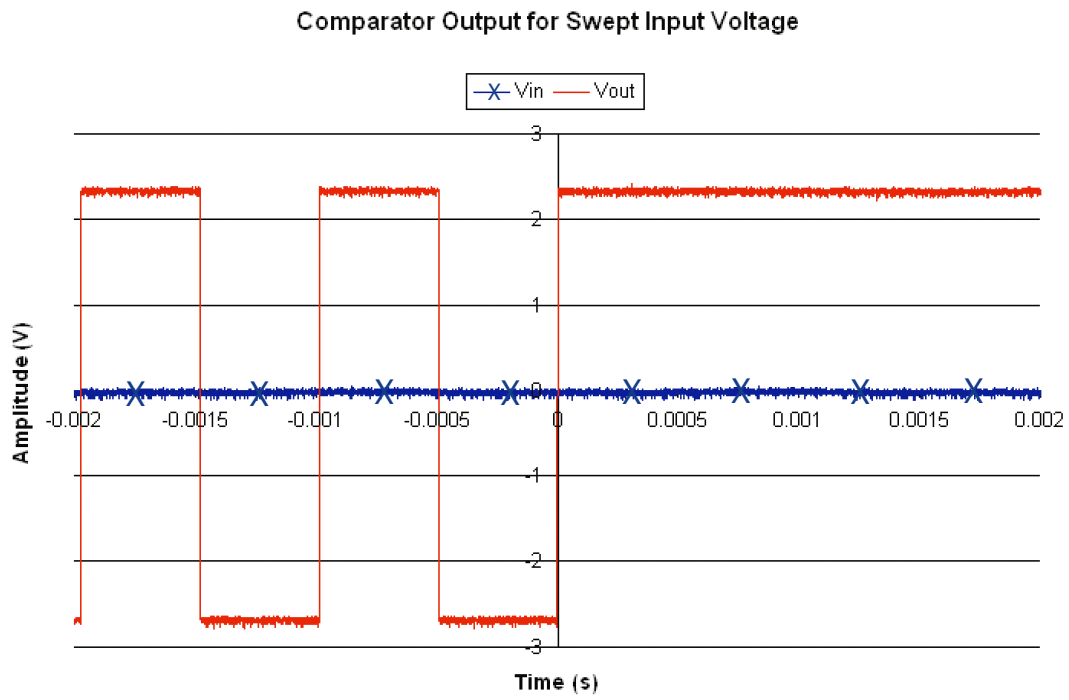
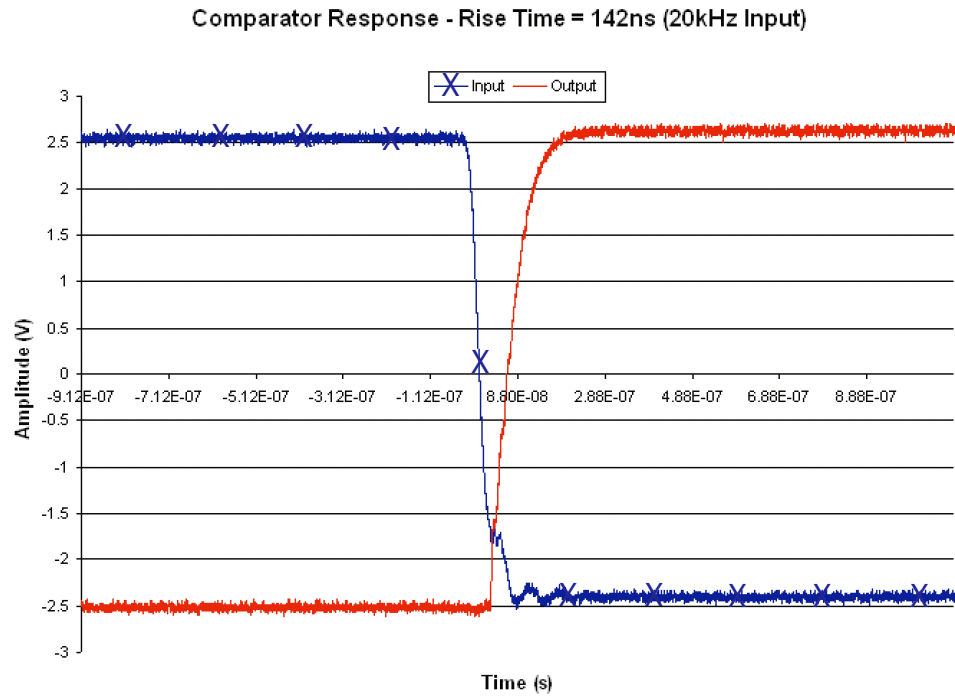Figure 9: Comparator sweep response
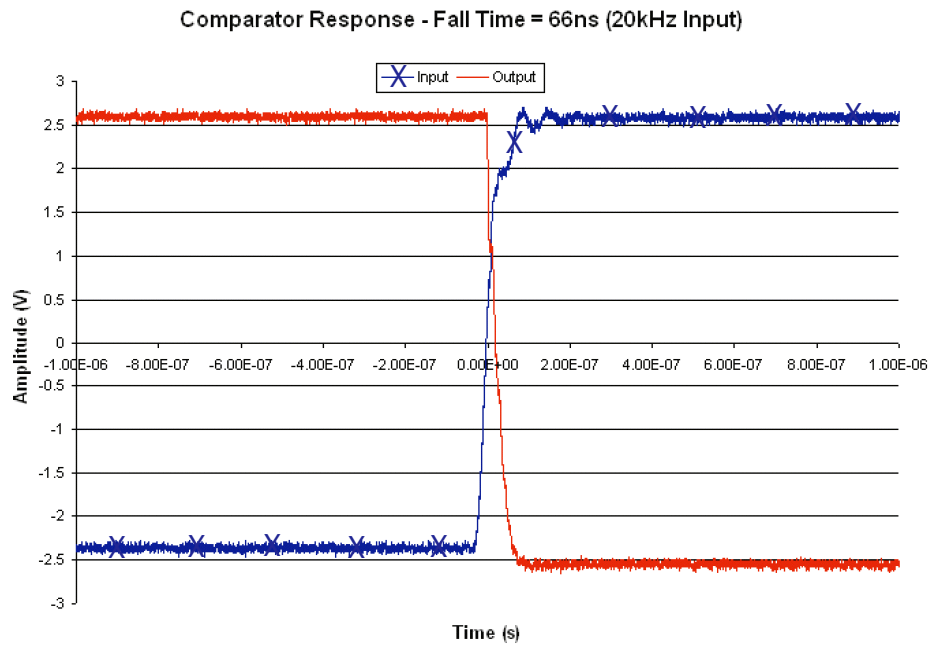
Figure 10: Comparator Rise Time

Figure 11: Comparator Fall Time

The current and power measurements for the comparator were taken under two separate conditions. Since the comparator is only activated when a predetermined number of samples have been integrated by the earlier components in the power sentry system, there are effectively two distinct states the comparator may be in. Either the comparator is sitting idle with a low latch signal while samples are integrated, or the comparator is deciding whether or not the integrated samples are above or below an applied threshold. For this reason, two separate power measurements were obtained for the comparator. While the comparator is in its idle state, it consumes 0.36nA of current, or a power of 1.8nW. When the comparator latch signal is asserted and the comparator determines the output, the circuit consumes 0.5nA of current, or a power of 2.5nW. Additionally, when the latch signal transitions from a low level to a high level, the comparator creates a current spike. As the frequency of these latch transitions increases, so does the average current consumption of the comparator. When the latch signal is transitioning at a frequency of 10kHz, the average current consumption of the comparator was measured to be I_{ave} = 0.76uA, which yields an average power of 3.8μW. This is an unlikely situation, though, since several samples must be taken before the integrator output is to be valid. Therefore, the average power consumption of the comparator is typically going to be less than 3.8μW.

Sentry System Test Results

The testing procedure is critical for determining whether or not the sentry system operates as expected. Figure (12) shows the entire power sentry system that is fabricated on the chip. The sampling capacitor, C_s, and feedback capacitor, C_f, are designed such that they can have values of either 1pF or 10pF. This allows for an integrator gain of 0.1, 1, or 10. The gain selection is controllable through two external pins (one for the sampling capacitor and the other for the feedback capacitor) that determine whether two internal capacitors (a 1pF and a 9pF) are added in parallel, resulting in a 10pF capacitance, or if only the 1pF capacitor is seen by the circuit.
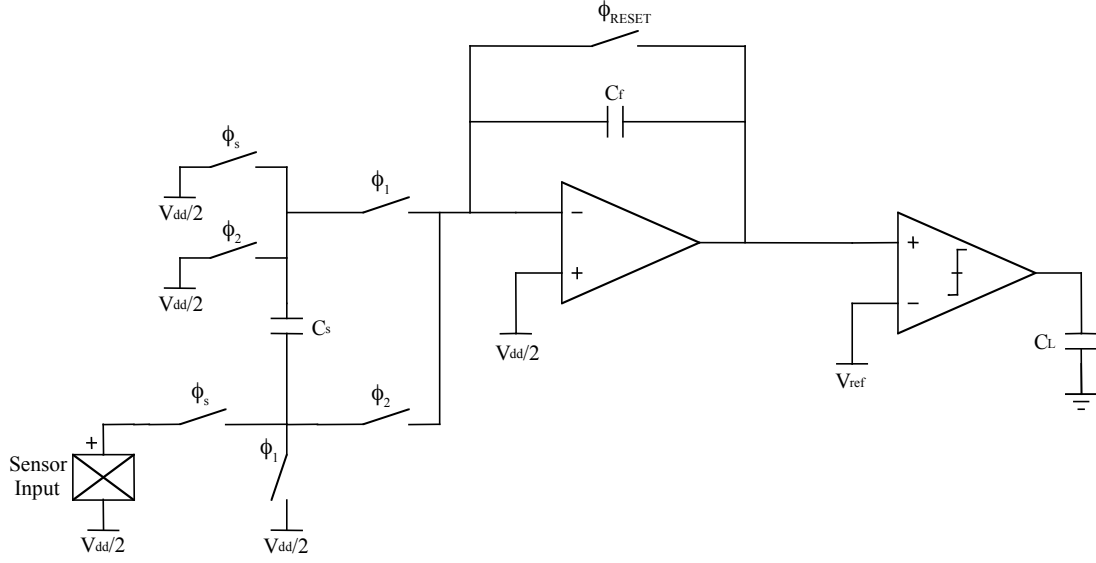
Figure 12: Power sentry system

The first simulation conducted on the power sentry system was for a purely DC input signal. For this test, the H_1 Hadamard basis function was selected so that the input voltage would be directly integrated without any sign alternations. The setup for this procedure is seen in Figure (13). Since the power sentry system is configured, in this case, to be a non-inverting integrator, the integrator output should increase for positive DC voltages until the integrator is reset, and the integrator output should decrease for negative DC voltages. The test circuit is set up so that the integrator gain is 0.1. This allows for more samples to be integrated before the latch signal is asserted. The latch signal tells the comparator to determine whether or not the output is valid. Since the integrator gain and sampling frequency are known and the DC input voltage is known and constant, the amount of time it takes until the integrator output validates can be explicitly calculated using Eq. (7), where f_{clk} = $2f_s$.

$$\Delta t = \frac{\left|V_{ref} - V_{in+}\right| \cdot 2}{\left|A_v\right| \cdot \left|V_{in}\right| \cdot f_{clk}} \tag{7}$$
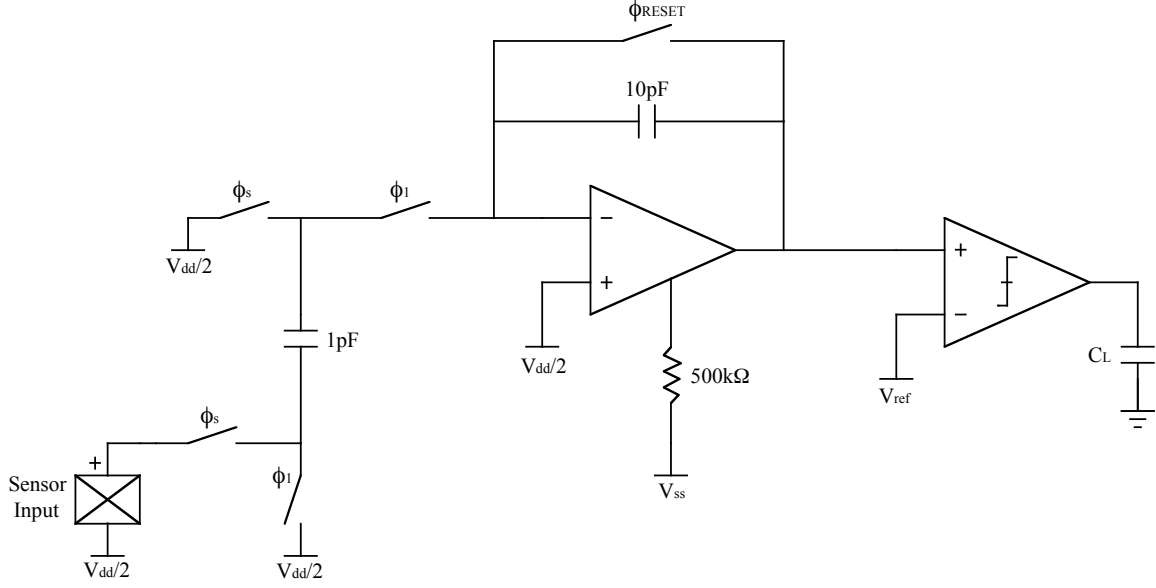
Figure 13: Sentry system test setup for DC case

The simulation setup for the DC voltage test is as follows. The supply voltages, V_{dd} and V_{ss} are 2.5V and –2.5V respectively. This places the $V_{dd}/2$ voltage at 0V, or ground. The comparator reference voltage, V_{ref}, depends on the input voltage. If a positive DC voltage is applied to the input, then V_{ref} is set to 1.25V. Alternatively, if the input voltage is a negative DC voltage, then V_{ref} is set to be –1.25V. This is due to the nature of the integrator output voltage. Since the integrator output increases for positive input voltages, a positive reference is used, and similarly, since the integrator output decreases for negative input voltages, a negative reference is used. Additionally, the clock signal is set to have a frequency of f_{clk} = 20kHz. To verify the integrator's functionality, four test results are shown. The first two are for positive input voltages of 0.1V and 0.4V. We can determine when to compare the integrator output to the reference through Eq. (7) shown above. For the 0.1V input, the latch signal is asserted at 13ms as shown in Fig. (14). Similarly, Fig. (15) shows the simulation result for the 0.4V input, where the latch signal is asserted at 3.2ms. The other two tests are for negative input voltages. The voltages used were –0.1V and –0.4V, which use the same latching times as their positive counterparts. Figures (16) and (17) show the results using the negative voltages of –0.1V and –0.4V respectively.
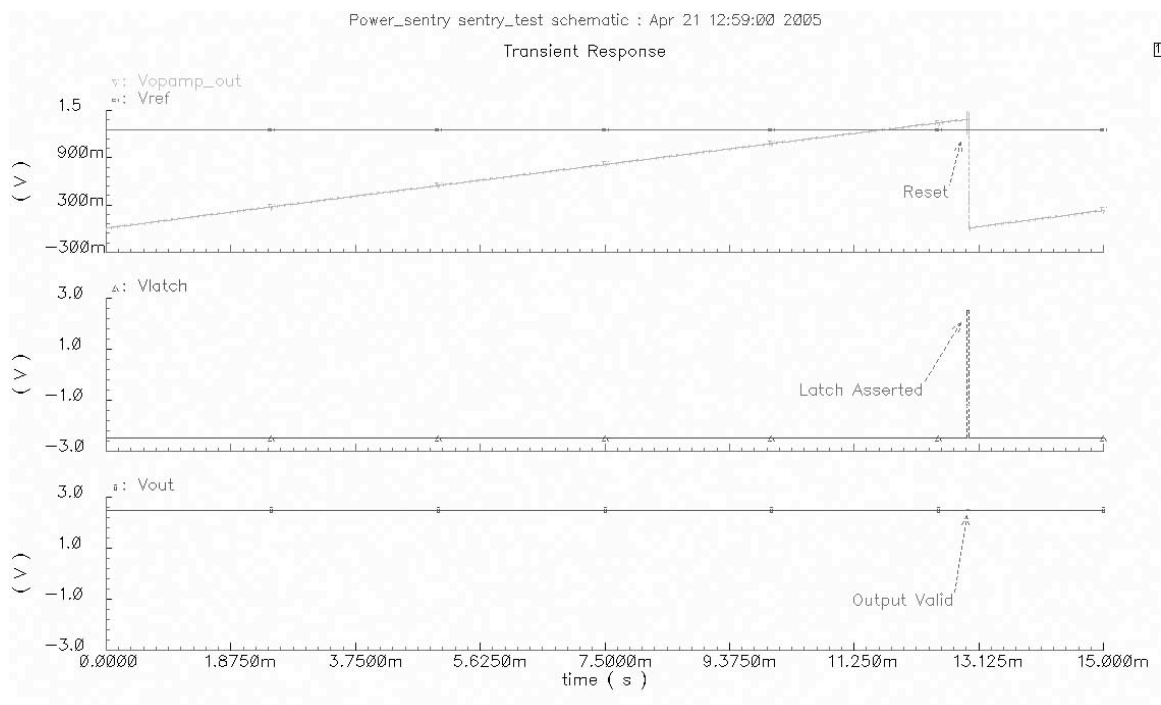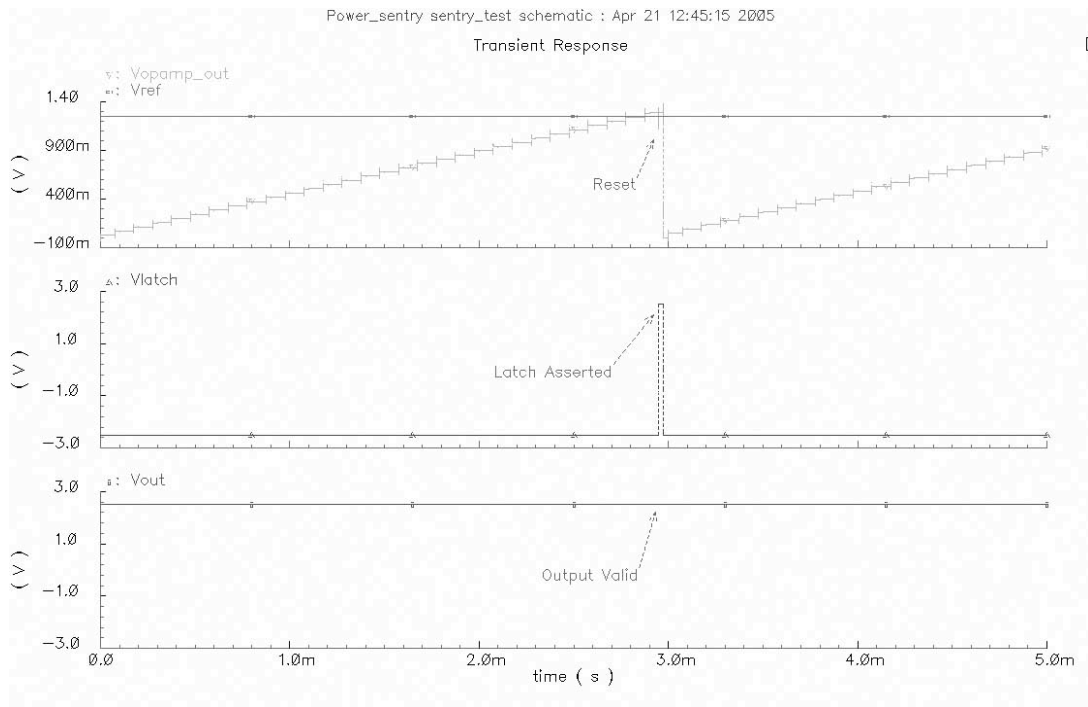
Figure 14: DC test with 0.1V input

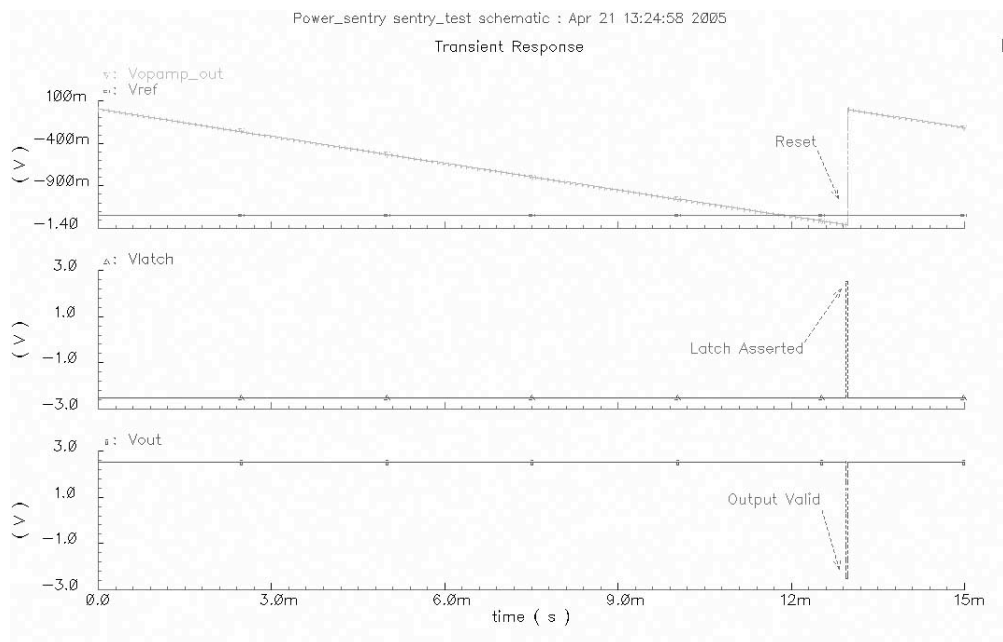Figure 15: DC test with 0.4V input

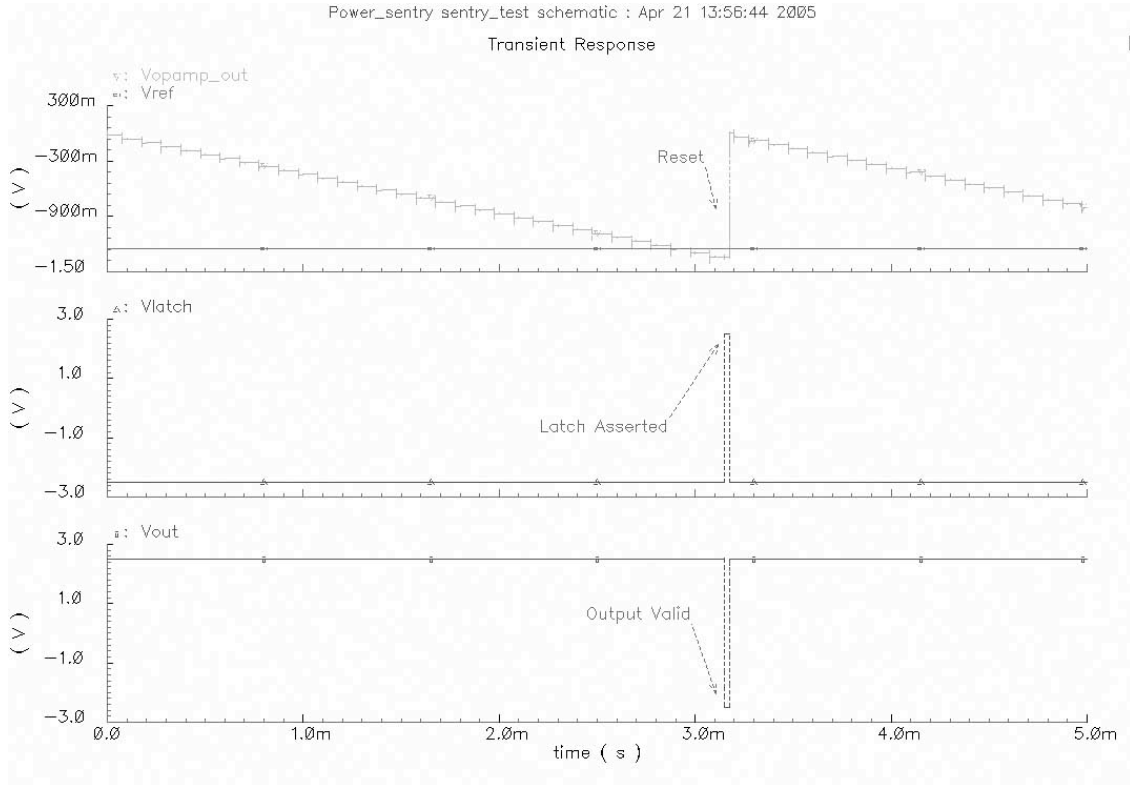

Figure 16: DC test with –0.1V input

Figure 17: DC test with -0.4V input

Once the sentry system operation was verified for a DC input through simulations, additional tests were conducted, including tests for Hadamard basis functions H_2 and H_3. The H_2 Hadamard basis function is used to detect $f_s/2$ frequencies, as stated previously. For the following simulation, f_s was set to be 10kHz, so H_2 should detect when a 5kHz signal is applied to the input. Several separate tests were conducted with different input frequencies in the range $0 < f_{in} < f_s$. Each simulation verified the circuit's functionality, and the particular results using f_{in} = 4kHz, 5kHz, and 6kHz are shown. The results from these simulations are shown below in Figures (18), (19), and (20), respectively. It is worth noting that for the simulations, V_{dd} = 2.5V, V_{ss} = -2.5V, $V_{dd}/2$ = 0V, and V_{ref} = 1.25V.

As seen in the figures, when the input frequency was set to 5kHz, the integrator output climbed above the comparator reference voltage, V_{ref}, which the comparator detected, forcing the power sentry system output to V_{dd} on the latch assertion. For the input

frequencies not equal to $f_s/2$, the integrator output fell below the comparator reference voltage, which forced the power sentry system output to V_{ss} when the latch signal was asserted. This switching nature of the output is due to the comparator design, which operates such that when V_{latch} is low, the comparator output is automatically pulled to V_{dd}. These simulation results verify that the use of Hadamard basis function, H_2, for detection of the $f_s/2$ frequency is valid.
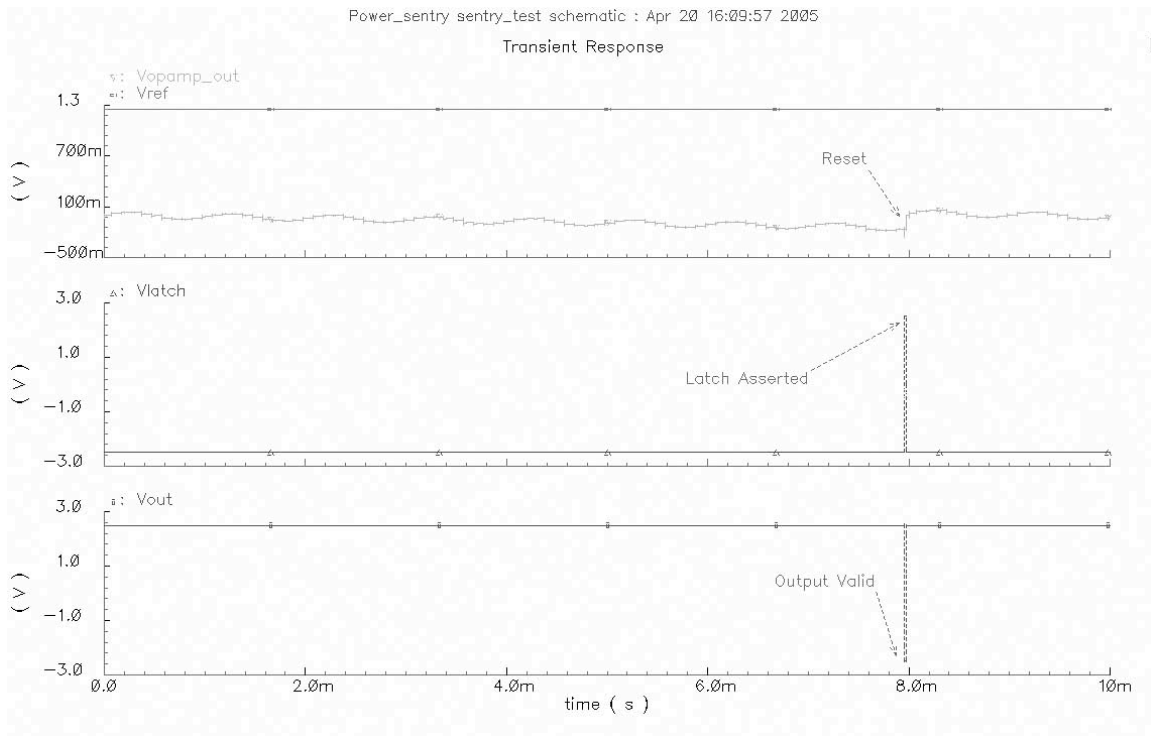

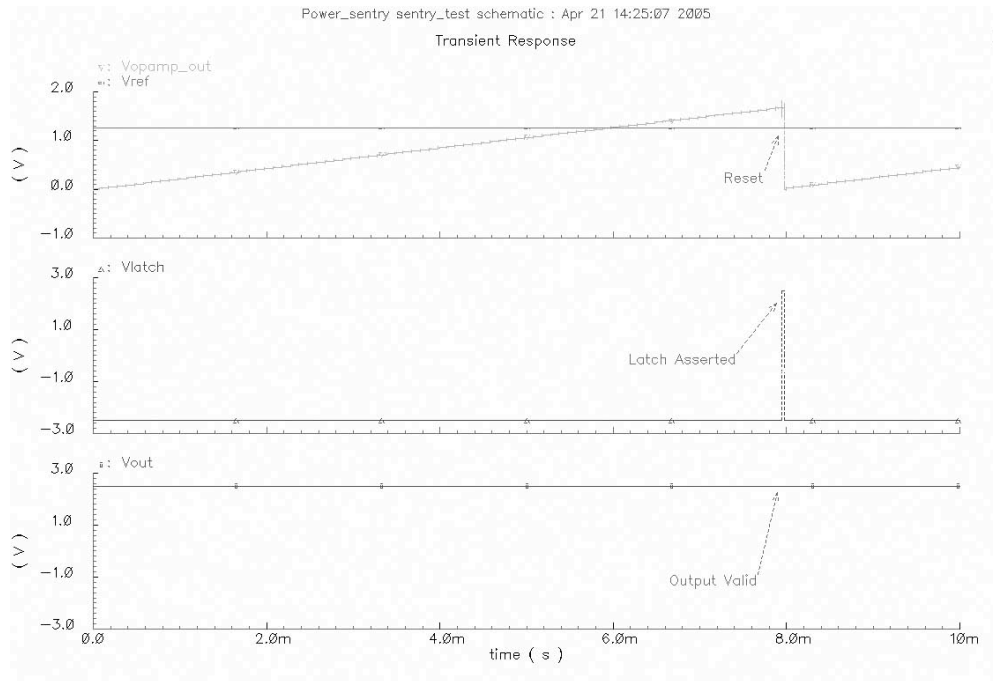Figure 18: Simulation results - H_2 with 4kHz input

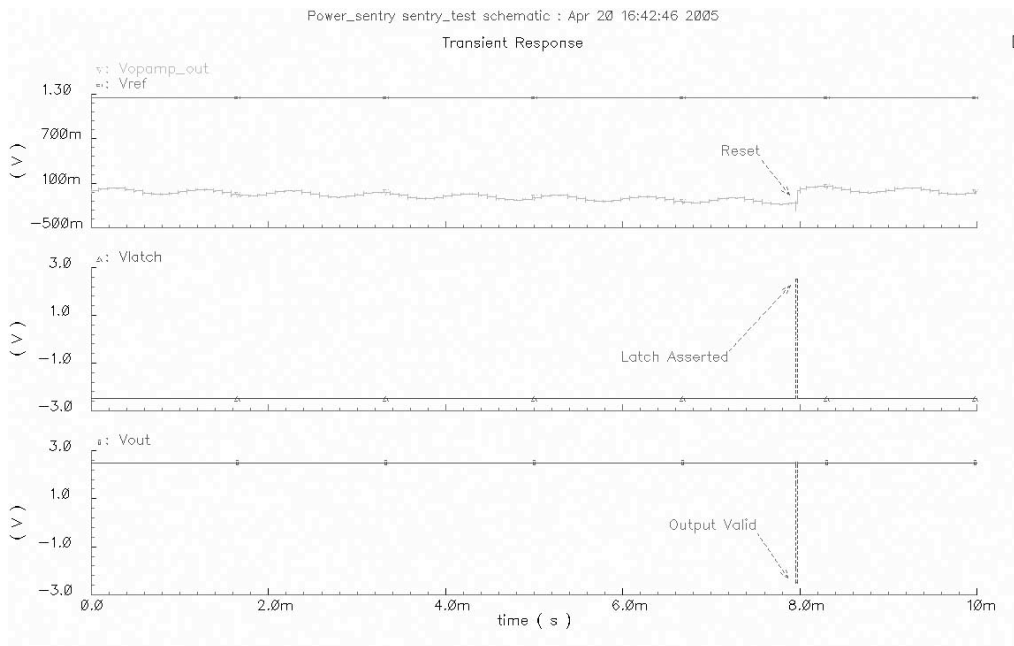Figure 19: Simulation results - H_2 with 5kHz input

Figure 20: Simulation results - H_2 with 6kHz input

The next test is for the H$_3$ Hadamard basis function, which is used to detect the f_s/4 frequency at the input to the power sentry system. As with the f_s/2 case, several simulations were executed with each verifying the circuit's functionality. To demonstrate this, three particular examples showing the results from f_{in} = 2kHz, 2.5kHz, and 3kHz are displayed. The simulation results are shown below in Figures (21), (22), and (23). The supply and reference voltage levels used for the simulations are the same as those used for the f_s/2 simulations and the input clock is the same.

The figures display very similar results to those seen for the f_s/2 frequency detection simulation. The power sentry system detects the presence of the f_s/4 frequency for the appropriate case, and also returns the proper results for the cases where the f_s/4 frequency is not applied to the power sentry system. As with the H$_2$ Hadamard basis function detection of f_s/2, the H$_3$ Hadamard basis function accurately detects the presence or absence of the f_s/4 frequency at the power sentry system's input.
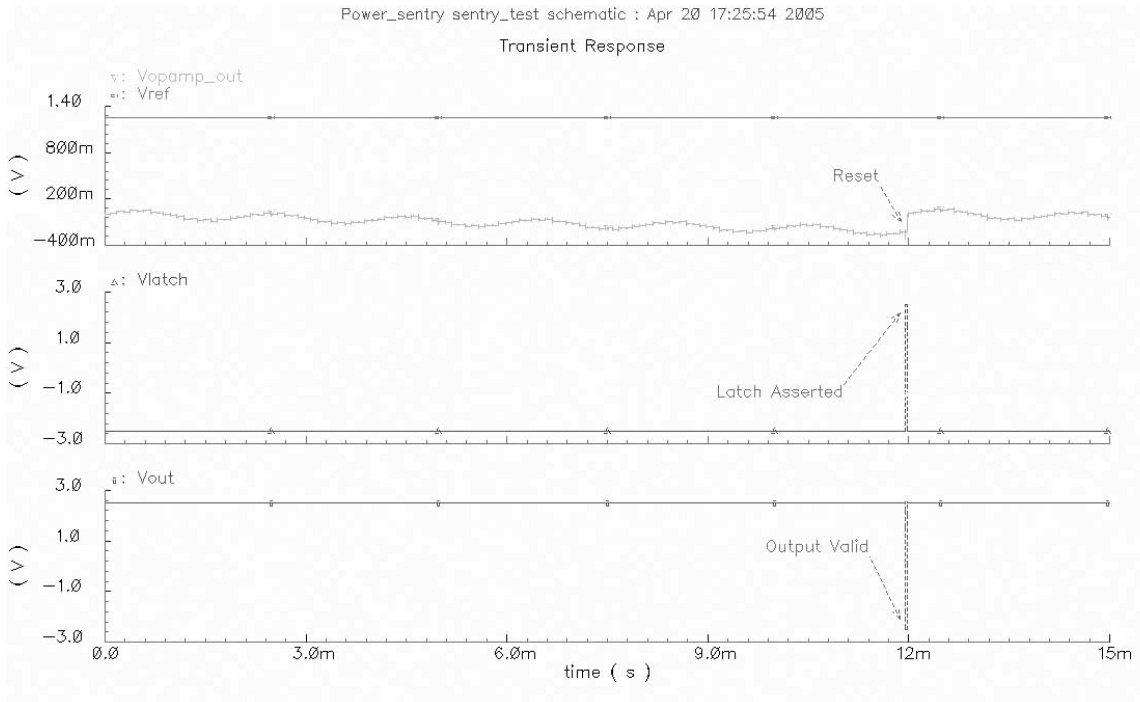

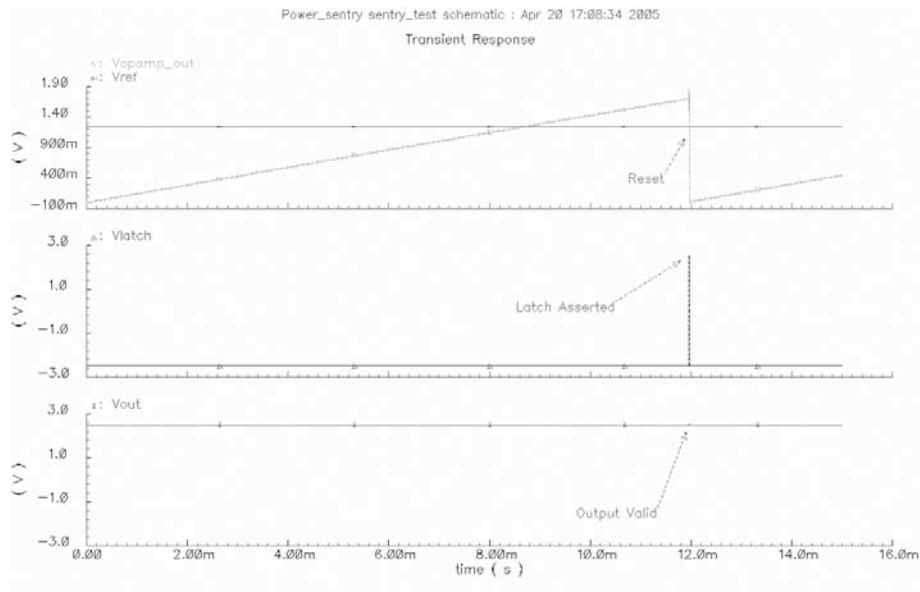Figure 21: Simulation results - H$_3$ with 2kHz input

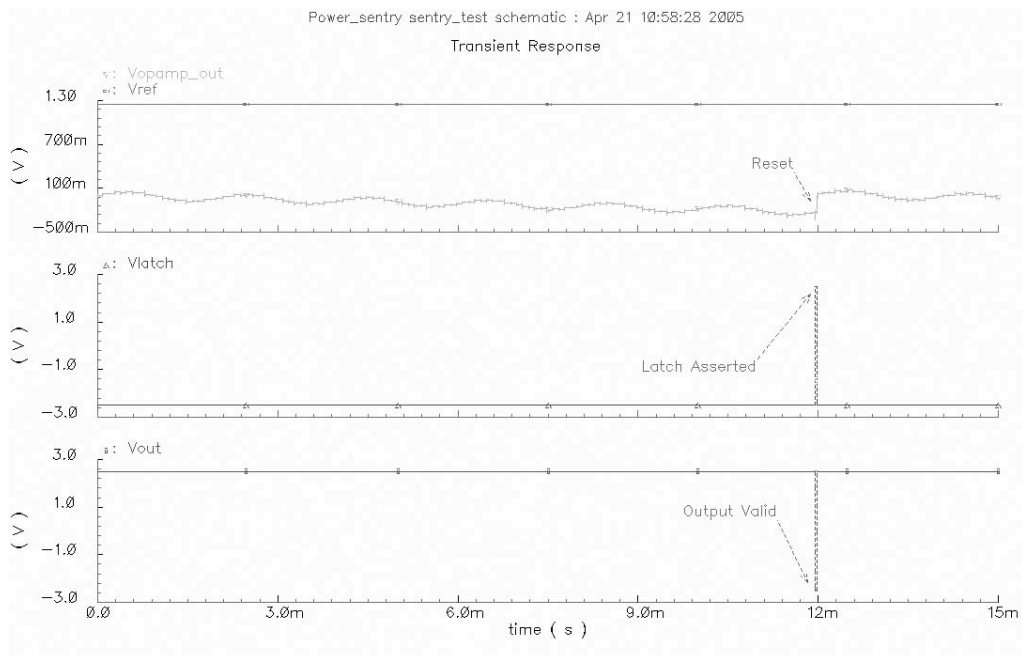Figure 22: Simulation results - H_3 with 2.5kHz input

Figure 23: Simulation results - H_3 with 3kHz input

The power sentry system's total current and power consumption will now be evaluated. Throughout the design and test process, this metric was continuously being considered. Table (3) presents the current and power consumption values for each individual component along with the total value for the entire system. The total provided is simply the sum of the current and power from each individual component, which is accurate since each circuit is functional individually and there are no additional components within the chip that would consume more power.

	Clock Generator	Op-amp	Comparator	Total
Current	0.274μA	2.645μA	0.76μA	3.668μA
Power	1.371μW	13.225μW	3.8μW	18.396μW

Table 3: Current and power for power sentry system

Since the simulation results for the power sentry system were rather promising, chip testing seemed as if it was going to be a straightforward task. Unfortunately, though, this was not the case. Despite verifying each of the component's functionality individually, when placed together in the sentry system structure, the behavior was unpredictable. Additionally, in the simulation environment, the reset and latching signals were very well defined; however, in reality, the signals were difficult to generate and control to ensure proper operation of the power sentry system. This led to the conclusion that feedback must be implemented in future designs to allow self-control of the reset function when any external latch signal is applied.

Following an analysis, it was determined that the reset function could be obtained through feedback for a specific testing case. When a negative DC voltage is applied at the power sentry input and a negative comparator reference voltage, V_{ref}, is used, the output will go low only when the integrator output crosses below the reference voltage and the latch

signal is asserted. As the simulations showed, this is an expected result for the described conditions. Additionally, since the sentry system resets on a digital '0', the output can be used to directly reset the system. This setup was used for the chip test, but the expected results were not seen. Instead, the output would irregularly cause the circuit to reset. These resets did not follow the results of Eq. (7) stated previously. For an input voltage of -0.1V, clock frequency f_{clk} = 2kHz, and integrator gain A_v = 0.1, the sentry system was expected to reset approximately every 125ms. Instead, the results were showing that the sentry system was resetting unpredictably in the range of 340ms to over 416ms. These unpredictable results were repeated throughout testing for the other input voltage values. Strangely, though, as the input voltage became more negative (i.e. a larger negative voltage was applied), the resets should have occurred more frequently as Eq. (7) predicts. However, in reality they remained close to the range of 340ms up to 416ms regardless of the input voltage being applied. It is believed that the integrator structure is experiencing a systematic offset error, which renders the integrator output insensitive to the input voltage values. After reexamining the circuit layout it was verified that even the slightest mismatch in the size of transistor M7 may lead to such a systematic error. This problem is more pronounced in single-ended designs.

For future designs of this system, it has been determined that a fully-differential integrator utilizing correlated double sampling (CDS) is necessary to cancel the problematic DC input offset voltage of the opamp, which is believed to be the major source of error with the present design. Such an integrator is seen in Figure (24) and is controlled by the clock sequence in Figure (25).

Figure 24: Correlated double sampling integrator

Figure 25: Clock sequence for CDS integrator

The reason for using a CDS integrator is that it effectively cancels the op-amp's input offset voltage. As seen in Figure (25), the integrator operates according to a non-overlapping two-phase clock. During the phase C_1, the input voltage is sampled to C_s and the op-amp's input offset voltage is sampled to C_{CDS}. Then, during phase C_2 the input voltage stored on C_s is transferred to C_f and the op-amp offset voltage is cancelled by the

charge stored on C_{CDS}. It should be noted that C_{1A} and C_{2A} should be opened slightly before C_1 and C_2, respectively, to reduce charge injection onto C_s.

Since the proposed integrator is a fully-differential design, the comparator used at the output must also be fully-differential. A fully-differential version of the comparator used for the initial design is shown in Figure (26) and is presented in [1]. This design has been shown to have a small area and power consumption, thus making it attractive for this application. Additionally, the design is insensitive to transistor mismatch.

Figure 26: Fully-differential comparator

These suggested improvements should help to eliminate the errors generated by the op-amp's input offset voltage that limited the performance of the presently designed power sentry system.

Reference:

[1] L. Sumanen, M. Waltari, and K. A. I. Halonen, "A mismatch insensitive CMOS dynamic comparator for pipeline A/D converters," in *Proc. ICECS*, vol. 1, Dec. 2000, pp. 32-35.